

P2004,0133

- 22 -

## Patent claims

1. A circuit arrangement for protecting an integrated semiconductor circuit comprising
  - 5 - a protection circuit, which contains a thyristor structure and is connected between an element to be protected and a reference potential,
  - a control circuit for driving the protection circuit,
- 10 characterized in that the control circuit (TC; C1, R1, I1 to I3) generates a plurality of control signals which in each case drive an active element (T1, T2) of the protection circuit (SCR).
- 15 2. The circuit arrangement as claimed in claim 1, characterized in that the control circuit contains a detector circuit (R1, C1), which, on the input side, is connected in parallel with the protection circuit and, in the case of a detection criterion being fulfilled,
- 20 drives switching elements (I1 to I3) which generate the control signals.
3. The circuit arrangement as claimed in claim 1 or 2, characterized in that the detector circuit contains
- 25 a first RC element (R1, C1) comprising a resistor and a capacitance.
4. The circuit arrangement as claimed in claim 2 or 3, characterized in that the switching elements contain
- 30 inverters (I1 to I3; I4 to I6).
5. The circuit arrangement as claimed in claims 1 to 4, characterized in that the control signals for active elements of different conductivity types of the
- 35 protection circuit are of opposite polarities and each drive a control input of the active elements.
6. The circuit arrangement as claimed in one of

P2004,0133

- 23 -

claims 1 to 5, characterized in that the detector circuit of the control circuit is designed for identifying a signal rise with a predetermined rise time at the element (PV, LV) to be protected.

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7. The circuit arrangement as claimed in one of claims 1 to 6, characterized in that the control circuit contains time-dependent elements (R1, C1; R10, C10, R20, C20) which determine the duration of the  
10 activation of the control circuit.

8. The circuit arrangement as claimed in claim 7, characterized in that the time-dependent elements are RC elements (R1, C1; R10, C10, R20, C20) which are  
15 crucial on the one hand for the beginning of the activation and on the other hand for the end of the activation of the control circuit.

9. The circuit arrangement as claimed in claim 2,  
20 characterized in that the detector circuit and the switching elements are embodied with individual transistors.

10. The circuit arrangement as claimed in claim 2 or  
25 9, the identification of a signal rise with a predetermined rise time at the element (PV, LV) to be protected being predetermined as a detection criterion of the control circuit.

30 11. The circuit arrangement as claimed in claim 9 or 10, the control circuit containing time-dependent elements (R13, C13; R10, C10, R20, C20) which determine the duration of the activation of the control circuit.

35 12. The circuit arrangement as claimed in one of patent claims 9 to 11, the detector circuit containing at least one RC element (R10, C10) comprising a resistor and a capacitance as time-dependent element

P2004,0133

- 24 -

and a detector switching element (TD10).

13. The circuit arrangement as claimed in one of patent claims 9 to 12, the connecting node between the  
5 detector circuit and the switching elements being connected to at least one further RC element (R30, C30), which is crucial for the duration of the activation of the control circuit.

10 14. The circuit arrangement as claimed in one of patent claims 9 to 13, the detector circuit being embodied from two detector subcircuits which in each case drive a switching element for the active elements of the protection circuit.

15 15. The circuit arrangement as claimed in one of patent claims 9 to 14, the switching elements being embodied as individual MOS or bipolar transistors (TH1, TL1; TH10, TL10).

20 16. The circuit arrangement as claimed in one of patent claims 9 to 15, driver elements (T12, T13) being connected upstream of the switching elements.

25 17. The circuit arrangement as claimed in one of claims 1 to 17, the control inputs of the active elements of the protection circuit being embodied in a semiconductor structure by means of wells of different conductivity types in which are arranged highly doped  
30 regions for the output circuits of the active elements (T1, T2).

18. A method for protecting an integrated semiconductor circuit with a circuit arrangement as  
35 claimed in one of patent claims 1 to 18, in which the state of the element (PV, LV) to be protected is detected and a control circuit (TC; C1, R1, I1 to I3) generates a plurality of control signals which are in

P2004,0133

- 25 -

each case fed to a control input of active elements  
(T1, T2) of the protection circuit.